UNIVERSITI MALAYA	**PRO FORMA KURSUS** ***COURSE PRO FORMA***

PENTING / *IMPORTANT*:

Kandungan Pro Forma ini tidak boleh diubah tanpa kelulusan Senat bagi perkara-perkara yang telah ditandakan*. Pindaan kepada perkara lain boleh diluluskan di peringkat Akademi/Fakulti/Institut/Pusat.

*Contents of this Pro Forma shall not be changed without the Senate's approval for items indicated with *. Changes to the other items can be approved at the Academy/Faculty/Institution/Centre level.*

	Versi Bahasa Malaysia ***Malay Version***	**Versi Bahasa Inggeris** ***English Version***
Akademi/Fakulti/Institut/Pusat *Academy/Faculty/Institute/Centre*	Fakulti Kejuruteraan	*Faculty of Engineering*
Jabatan *Department*	Jabatan Kejuruteraan Elektrik	*Department of Electrical Engineering*
Nama Program Akademik Name of Academic *Programme*	Sarjana Muda Kejuruteraan (Elektrik)	*Bachelor of Engineering (Electrical)*
Kod Kursus* *Course Code**	KIE4019	*KIE4019*
Tajuk Kursus* *Course Title**	Rekabentuk Litar VLSI Analog	*Analog VLSI Circuit Design*
Kredit* *Credit**	2	*2*
Masa Pembelajaran Pelajar (SLT) *Student Learning Time (SLT)*	80	*80*
Prasyarat/Keperluan Minimum Kursus *Course Pre-requisite(s)/Minimum Requirement(s)*	-	-
Hasil Pembelajaran Kursus* *Course Learning Outcomes**	Di akhir kursus ini, pelajar dapat: 1) Menganalisis konsep teori litar VLSI CMOS analog. 2) Mengintegrasi litar CMOS analog asas. 3) Menilai prestasi litar terkamil analog CMOS mengadaptasikan perisian komputer canggih.	*At the end of the course, students are able to:* *1) Analyze the theoretical concepts of analog CMOS VLSI circuits.* *2) Integrate basic analog CMOS VLSI circuits.* *3) Evaluate the performance of integrated CMOS analog circuits adapting standardized state of the art tools.*

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Kemahiran Insaniah *Soft Skills*	Kemahiran Pemikiran Kritis dan Penyelesaian Masalah (CT1-CT3)	*Critical Thinking and Problem Solving Skills (CT1-CT3)*
Sinopsis Kandungan Kursus *Synopsis of Course Contents*	Kursus ini berperanan dalam memperkenalkan konsep pemodelan ,merekabentuk dan analisis litar CMOS VLSI analog. Pelajar dilengkapi dengan teori latarbelakang litar terkamil analog yang kukuh berdasarkan analisis rekabentuk masing-masing. Mempertimbangkan parameter praktikal, litar arus cermin, penguat pembezaan, kesaksamaan voltan/arus rujukan dan litar analog ketaklurusan direkabentuk mengadaptasikan faedah dan batasan masing-masing. Pelajar didedahkan dalam pengunaan perisian EDA bertahap industri dalam tujan merekabentuk, mempertingkatkan dan simulasi litar terkamil CMOS analog.	*The goal of this course is to introduce the modelling, design and analysis of analog CMOS VLSI circuits. A strong theoretical background of integrated analog circuits design is imparted to the students along with the emphasis on their design and analysis. Design of CMOS based current mirrors, integrated differential amplifiers, precision voltage/current reference and nonlinear analog circuits are discussed considering practical parameters, adapting their advantages and limitations. Students will be exposed to use industry standard EDA tools to design, optimize and simulate analog CMOS integrated circuits.*
Pemberatan Penilaian* *Assessment Weightage**	Penilaian Berterusan: 40% Peperiksaan Akhir: 60%	*Continuous Assessment: 40%* *Final Examination: 60%*
Kaedah Maklum Balas Tentang Prestasi *Methodologies for Feedback on Performance*	Gred/markah untuk tugasan, ujian dan/atau pembentangan individu diumumkan dalam kelas dan/atau dipamerkan di papan kenyataan.	*Grades/marks for assignment, test and/or individual presentation announced in class and/or displayed on the notice board*
Kriteria Dalam Penilaian Sumatif *Criteria in Summative Assessment*	Sila rujuk Kaedah-Kaedah Universiti Malaya (Pengajian Ijazah Pertama) 2017 dan Peraturan-Peraturan Universiti Malaya (Pengajian Ijazah Pertama) 2017	*Please refer to the University Of Malaya (First Degree Studies) Rules 2017 And University Of Malaya (First Degree Studies) Regulations 2017*